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Confirmation No. 4584

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	MUTH	Examiner:	Amrany, Adi
Serial No.:	10/511,492	Group Art Unit:	2836
Filed:	October 15, 2004	Docket No.:	DE020097US (NXPS.266PA)
Title:	CIRCUIT ARRANGEMENT FOR GENERATING DC VOLTAGES		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being transmitted via facsimile-Formal Entry, to the attention of the Examiner at Commissioner for Patents, MAIL APPEAL BRIEFS, P.O. Box 1450, Alexandria, VA 22313-1450, on March 15, 2010

By: Kelly J. Davis
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APPEAL BRIEF

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Commissioner For Patents
P.O. Box 1450
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Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed January 14, 2010 and in response to the rejections of claims 1-17 as set forth in the Final Office Action dated October 22, 2009.

Please charge Deposit Account No. 50-4019 (DE020097US) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-4019 additional fees/overages in support of this filing.

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I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-17 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated October 22, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a circuit arrangement for a vehicle for generating at least two DC output voltages from at least one DC input voltage, wherein the DC output voltages are

smaller than the DC input voltage, the circuit arrangement comprising: a voltage regulator for generating the DC output voltages, to supply operating power to a set of circuit elements used for operating the vehicle, from a voltage regulator input (*see, e.g.*, voltage regulators 3 and 4 shown in Fig. 1 and page 3:23-29), a DC/DC converter for converting the DC input voltage to a lower voltage, the DC/DC converter configured to be switched on or off responsive to an on-off signal and to supply the lower voltage to the voltage regulator input as a source for generating the DC output voltages (*see, e.g.*, voltage converter 2 shown in Fig. 1 and page 3:19-22), and a logic circuit configured to provide the on-off signal to the DC/DC converter in response to an idle state in which the set of circuit elements are switched off, the logic circuit further configured to receive the DC input voltage to power the logic circuitry when the DC/DC converter is switched off (*see, e.g.*, control circuit 5 shown in Fig. 1 and page 3:30 to page 4:16).

Commensurate with independent claim 5, an example embodiment of the present invention is directed to an integrated circuit for a vehicle for generating DC output voltages from at least one DC input voltage, wherein the DC output voltages are smaller than the DC input voltage, the integrated circuit comprising: a voltage regulator for generating the DC output voltages from a voltage regulator input (*see, e.g.*, voltage regulators 3 and 4 shown in Fig. 1 and page 3:23-29); an on-off logic circuit configured to generate a switching signal in response to an idle state in which circuit elements powered by the DC output voltages are off, the circuit elements used for operating the vehicle, the on-off logic circuit further configured to receive the DC input voltage to power the on-off logic circuit (*see, e.g.*, control circuit 5 shown in Fig. 1 and page 3:30 to page 4:16); and a DC/DC converter configured to switch on or off in response to the switching signal (*see, e.g.*, voltage converter 2 shown in Fig. 1 and page 3:19-22).

Commensurate with independent claim 13, an example embodiment of the present invention is directed to a circuit arrangement for a vehicle, the circuit arrangement comprising: a DC/DC converter configured to convert a DC input voltage to a lower voltage responsive to an on-off signal (*see, e.g.*, voltage converter 2 shown in Fig. 1 and page 3:19-22); a voltage regulator configured to generate at least two DC output voltages from the lower voltage and to supply the DC output voltages to circuit elements used for operating the

vehicle, the DC output voltages being smaller than the DC input voltage (*see, e.g.*, voltage regulators 3 and 4 shown in Fig. 1 and page 3:23-29); and control circuitry configured to generate the on-off signal responsive to an idle state in which the circuit elements are switched off, the control circuitry including an input that is configured to receive the DC input voltage to power the control circuitry (*see, e.g.*, control circuit 5 shown in Fig. 1 and page 3:30 to page 4:16).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

Claims 1-17 stand rejected under 35 U.S.C. § 103(a) over Applicant's admitted prior art ("APA", specification, page 1) in view of Kawaguchi (U.S. Patent No. 5,793,189).

VII. Argument

A. The § 103(a) Rejection Of Claims 1-17 Is Improper Because The Cited References Fail To Disclose A Logic Circuit That Is Powered By The Same DC Input Voltage That A DC/DC Converter Converts To A Lower Voltage.

The cited references do not correspond to the claimed invention. For example, neither APA nor the '189 reference teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.*, a logic circuit that provides an on-off signal to a DC/DC converter and that is powered by the same DC input voltage that the DC/DC converter converts to a lower voltage. Because none of the references teach the above discussed aspects, no reasonable combination of these references can provide correspondence to the claimed invention. In particular, the '189 reference teaches that voltage VJ (*i.e.*, the asserted voltage the DC/DC converter converts to a lower voltage) is not the same as voltage VK (*i.e.*, the asserted voltage that powers the logic circuit). *See, e.g.*, Fig. 1. As the Examiner's rejection expressly relies upon the erroneous conclusion that the voltages VJ and VK in the '189 reference are the same, the § 103(a) rejection necessarily fails.

More specifically, the Examiner acknowledges that APA does not teach a logic circuit as in the claimed invention (*see, e.g.*, page 4 of the Office Action dated October 22, 2009). Appellant submits that the '189 reference also fails to teach such a logic circuit.

Instead, the Examiner bases the rejection upon an improper interpretation of the teachings of the '189 reference. In pertinent part, the Examiner's rejection relies upon the erroneous assertion that the voltage provided at HVI (*i.e.*, the asserted DC input voltage) is the same as the voltage provided to input terminal ST (*i.e.*, the asserted logic circuit) because the voltage provided at HVI is equal to voltage VJ minus the voltage drop of diode 16 and the voltage provided to input terminal ST is equal to voltage VK minus the voltage drop of diode 18 (*see, e.g.*, Figure 1). The Examiner's assertion, however, is premised upon the erroneous conclusion that the voltages VJ and VK at each of the corresponding diodes 16 and 18 are the same. The '189 reference clearly teaches that this is not the case. For example, circuit 17 in Fig. 1 of the '189 reference is a voltage regulating circuit that changes the voltage VJ from a relatively high voltage to a relatively low voltage VK. *See, e.g.*, the Zener diode in circuit 17, which is used as a voltage regulator. The '189 reference explains this at Col. 6:51-56: "(t)he charge interface (I/F) circuit 11 includes a simplified constant voltage circuit 17...The simplified constant voltage circuit 17 outputs a DC voltage VK required for starting the DC-DC converter 6." It should therefore be clear that the Examiner's conclusion regarding the voltages VJ and VK being the same is erroneous. As such, the '189 reference does not teach that the same DC input voltage is provided to both the HVI of converter 6 (*i.e.*, the asserted DC/DC converter) and the input terminal ST (*i.e.*, the asserted logic circuit), as in the claimed invention. Accordingly, the Examiner's proposed combination of APA and the '189 reference does not correspond to the claimed invention.

Moreover, the Examiner's assertion in the Advisory Action that "It would be obvious to one of skill in the art that the voltage provided to the ST terminal is sufficient to power the logic circuit" is irrelevant because the Examiner's assertion fails to address the actual claim limitations which require that the voltage that powers the logic circuit be the same as the voltage that the DC/DC converter converts to a lower voltage. In the '189 reference, the voltage VK is not the same as the voltage VJ as discussed above, and, as such, the rejection necessarily fails.

In view of the above, the § 103(a) rejection claims 1-17 is improper and Appellant requests that it be reversed.

B. The § 103(a) Rejection Of Claims 1-17 Is Improper Because The Cited References Fail To Disclose A Logic Circuit That Receives A DC Input Voltage To Power The Logic Circuit When A DC/DC Converter Is Off.

Neither APA nor the '189 reference teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.*, a logic circuit that is configured to receive the same DC input voltage, which a DC/DC converter converts to a lower voltage, to power the logic circuit when the DC/DC converter is switched off. In particular, the Examiner improperly bases the rejection upon aspects of two mutually exclusive embodiments of Fig. 1 of the '189 reference. The Examiner expressly relies upon an embodiment of Fig. 1 of the '189 reference in which voltage VK is provided to input terminal ST of converter 6 (*see, e.g.*, page 4 of the Office Action dated October 22, 2009). The '189 reference teaches that the DC/DC converter 6 is always on when the voltage VK is provided (via charger 10). As such, this embodiment of the '189 reference does not correspond to the claimed invention. As the Examiner has expressly relied upon the embodiment of Fig. 1 of the '189 reference in which the charger 10 is connected and in which the converter 6 is necessarily switched on, the Examiner's further reliance upon another embodiment of Fig. 1 of the '189 reference in which the converter 6 is off when the charger 10 is not connected is improper. Thus, the Examiner's reliance upon two mutually exclusive embodiments of Fig. 1 of the '189 reference is improper and the § 103(a) rejection necessarily fails.

More specifically, the Examiner acknowledges that APA does not teach the logic circuit of the claimed invention (*see, e.g.*, page 4 of the Office Action dated October 22, 2009). Appellant submits that the '189 reference also fails to teach such a logic circuit. Instead, the circuit of the '189 reference is designed such that anytime the charger 10 outputs the charging DC power VJ, the DC/DC converter 6 (*i.e.*, the asserted DC/DC converter) is also on because the input terminal ST (*i.e.*, the asserted logic circuit) is active high. For example, the constant voltage circuit 17 in Fig. 1 of the '189 reference always outputs the voltage VK, which is supplied to the input terminal ST to start the converter 6, when the charging power VJ is provided (*see, e.g.*, Col. 6:40-65). Thus, there is no situation in which the input terminal ST of the '189 reference receives the voltage VK and the DC/DC converter 6 is switched off (*i.e.*, if the voltage VK is present, the DC/DC converter 6 is

necessarily switched on). Accordingly, the Examiner's proposed combination of APA and the '189 reference does not correspond to the claimed invention.

In view of the above, the § 103(a) rejection claims 1-17 is improper and Appellant requests that it be reversed.

C. The § 103(a) Rejection Of Claims 1-17 Is Improper Because The Cited References Fail To Disclose A Logic Circuit Configured To Provide An On-Off Signal To A DC/DC Converter In Response To An Idle State.

Neither APA nor the '189 reference teach the claimed invention "as a whole" (§ 103(a)) including, *e.g.*, a logic circuit that is configured to provide an on-off signal to a DC/DC converter in response to an idle state in which a set of circuit elements powered by the DC/DC converter are switched off. In particular, the Examiner improperly bases the rejection upon aspects of two mutually exclusive embodiments of Fig. 1 of the '189 reference. The Examiner expressly relies upon an embodiment of Fig. 1 of the '189 reference in which voltage VK is provided to input terminal ST of converter 6 (*see, e.g.*, page 4 of the Office Action dated October 22, 2009). The '189 reference teaches that the DC/DC converter 6 is always on when the voltage VK is provided (via charger 10). As the Examiner has expressly relied upon the embodiment of Fig. 1 of the '189 reference in which the charger 10 is connected and in which the converter 6 is necessarily switched on, the Examiner's further reliance upon another embodiment of Fig. 1 of the '189 reference in which the converter 6 is turned on or off in response to a battery voltage level (*e.g.*, for protecting against over-discharge of the battery) when the charger 10 is not connected is improper. Appellant submits that the converter 6 does not respond to the battery voltage level when the charger 10 is connected. Accordingly, the Examiner's reliance upon two mutually exclusive embodiments of Fig. 1 of the '189 reference is improper and the § 103(a) rejection necessarily fails.

More specifically, the Examiner acknowledges that APA does not teach a logic circuit as in the claimed invention (*see, e.g.*, page 4 of the Office Action dated October 22, 2009). Appellant submits that the '189 reference also fails to teach such a logic circuit. In particular, the Examiner fails to address claimed limitations directed to the on/off signal and the responsiveness to an idle state. The Examiner hypothesizes that the DC/DC converter 6

in Fig. 1 of the '189 reference may be on or off when various circuit elements are also on or off; however, the Examiner stops short of presenting evidence of how the DC/DC converter of the '189 reference is responsive to an idle state. Appellant submits that the '189 reference teaches that the DC/DC converter 6 is turned on or off in response to a battery voltage level for the express purpose of protecting against over-discharge of the battery. Thus, the only aspect that the DC/DC converter 6 is taught to respond to is a battery voltage level. Appellant submits that it is not possible to know whether the DC/DC converter 6 of the '189 reference is on or off when looking at the state of the circuits identified by the Examiner because the control aspect of the converter 6 is the battery charge level. The skilled artisan would readily understand that the DC/DC converter 6 is in no reasonable way responsive to any idle state. Instead, the DC/DC converter 6 is expressly and only responsive to a battery charge level. This is easily confirmed by a brief review of the relevant figures and associated description of the '189 reference. Accordingly, the Examiner's rejection fails to show correspondence to each element of the claimed invention as required.

In view of the above, the § 103(a) rejection claims 1-17 is improper and Appellant requests that it be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-17 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/511,492)

1. A circuit arrangement for a vehicle for generating at least two DC output voltages from at least one DC input voltage, wherein the DC output voltages are smaller than the DC input voltage, the circuit arrangement comprising:

a voltage regulator for generating the DC output voltages, to supply operating power to a set of circuit elements used for operating the vehicle, from a voltage regulator input,

a DC/DC converter for converting the DC input voltage to a lower voltage, the DC/DC converter configured to be switched on or off responsive to an on-off signal and to supply the lower voltage to the voltage regulator input as a source for generating the DC output voltages, and

a logic circuit configured to provide the on-off signal to the DC/DC converter in response to an idle state in which the set of circuit elements are switched off, the logic circuit further configured to receive the DC input voltage to power the logic circuitry when the DC/DC converter is switched off.

2. A circuit arrangement as claimed in claim 1, characterized in that the DC input voltage is used for energy supply of the arrangement.

3. A circuit arrangement as claimed in claim 1, characterized in that, with the exception of the DC/DC converter, the circuit arrangement is realized on an integrated circuit which is preceded by the DC/DC converter.

4. A circuit arrangement as claimed in claim 1, characterized in that the circuit arrangement is realized together with the DC/DC converter on an integrated circuit.

5. An integrated circuit for a vehicle for generating DC output voltages from at least one DC input voltage, wherein the DC output voltages are smaller than the DC input voltage, the integrated circuit comprising:

a voltage regulator for generating the DC output voltages from a voltage regulator input;

an on-off logic circuit configured to generate a switching signal in response to an idle state in which circuit elements powered by the DC output voltages are off, the circuit elements used for operating the vehicle, the on-off logic circuit further configured to receive the DC input voltage to power the on-off logic circuit; and

a DC/DC converter configured to switch on or off in response to the switching signal.

6. A circuit arrangement as claimed in claim 1, characterized in that the DC input voltage has a value of approximately 42 volts and the voltage supplied by the DC/DC converter has a value of approximately 12 volts.

7. The circuit arrangement of claim 1, wherein the logic circuit is not powered by the DC/DC converter when the DC/DC converter is on.

8. The circuit arrangement of claim 1, wherein the DC output voltages are smaller than the lower voltage.

9. The circuit arrangement of claim 1, further comprising a power supply configured to supply the DC input voltage, and wherein the circuit arrangement does not include a battery that is separate from the power supply.

10. The integrated circuit of claim 5, further comprising a power supply configured to supply the DC input voltage, wherein the integrated circuit does not include a battery that is separate from the power supply, and wherein the on-off logic circuit is not powered by the DC/DC converter when the DC/DC converter is on.

11. The integrated circuit of claim 5, wherein the DC/DC converter is configured to convert the DC input voltage to a lower voltage and to supply the lower voltage to the voltage regulator input.

12. The integrated circuit of claim 11, wherein the DC output voltages are smaller than the lower voltage.

13. A circuit arrangement for a vehicle, the circuit arrangement comprising:

a DC/DC converter configured to convert a DC input voltage to a lower voltage responsive to an on-off signal;

a voltage regulator configured to generate at least two DC output voltages from the lower voltage and to supply the DC output voltages to circuit elements used for operating the vehicle, the DC output voltages being smaller than the DC input voltage; and

control circuitry configured to generate the on-off signal responsive to an idle state in which the circuit elements are switched off, the control circuitry including an input that is configured to receive the DC input voltage to power the control circuitry.

14. The circuit arrangement of claim 13, wherein the control circuitry is not powered by the DC/DC converter when the DC/DC converter is on.

15. The circuit arrangement of claim 13, wherein the DC output voltages are smaller than the lower voltage.

16. The circuit arrangement of claim 13, further comprising a power supply configured to supply the DC input voltage, and wherein the circuit arrangement does not include a battery that is separate from the power supply.

17. The circuit arrangement of claim 13, wherein the DC/DC converter is configured to turn off responsive to the on-off signal when the circuit elements are to be turned off and the

DC/DC converter is configured to turn on responsive to the on-off signal when the circuit elements are to be turned on.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.